CLAIMS

We claim:

1. A process for forming at least one interface region between two regions of semiconductor material, the process comprising:

forming at least one region of dielectric material comprising nitrogen in the vicinity of at least a portion of a boundary between the two regions of semiconductor material, thereby controlling electrical resistance at the interface.

2. The process according to claim 1, wherein the two regions of semiconductor material each are selected from the group consisting of monocrystalline silicon, polycrystalline silicon, amorphous silicon, monocrystalline SiGe and polycrystalline SiGe.

3. The process according to claim 1, wherein a first of the two regions of semiconductor material is monocrystalline silicon and a second of the regions of semiconductor material is non-monocrystalline silicon.

4. The process according to claim 3, wherein the second region of semiconductor material is amorphous silicon.

5. The process according to claim 1, wherein the dielectric material is N, Si_xN_y, or $Si_xO_yN_z$.

6. The process according to claim 1, wherein forming the at least one region of dielectric material comprises:

implanting the dielectric material in the vicinity of the surface of a first of the regions of semiconductor material.

7. The process according to claim 6, wherein the dielectric material is deposited at an energy sufficient to create a discontinuous layer of dielectric material.

8. The process according to claim 6, wherein the dielectric material is deposited at a thickness and covering a portion of the boundary between the two regions of semiconductor material sufficient to control base current flowing between the two regions of semiconductor material.

9. The process according to claim 6, wherein the

dielectric material is implanted at the surface of the first region of semiconductor material.

10. The process according to claim 6, wherein atoms or molecules of the dielectric material are implanted at the surface of one of the regions of semiconductor material.

11. The process according to claim 6, wherein atoms or molecules of the dielectric material are implanted under the surface of one of the regions of semiconductor material.

12. The process according to claim 6, wherein one of the regions of semiconductor material is monocrystalline silicon and the dielectric material includes nitrogen atoms implanted in the monocrystalline silicon.

13. The process according to claim 12, wherein the nitrogen atoms are implanted at an energy of about 0.1 KeV to about 5 KeV.

14. The process according to claim 12, wherein the nitrogen atoms are implanted at a dose of from about 1×10^{11} to about 1×10^{14} and with an energy of about 0.1 KeV to about 5 KeV.

15. The process according to claim 6, further comprising:

subjecting the semiconductor material and the implanted dielectric material to an annealing step.

16. The process according to claim 6, further comprising:

utilizing a mask to selectively implant the dielectric material in the semiconductor.

17. The process according to claim 6, further comprising:

implanting a layer of the dielectric material; and

selectively removing portions of the dielectric material.

18. The process according to claim 1, wherein forming the at least one region of dielectric material comprises:

subjecting a first of the regions of semiconductor material to a elevated temperatures and a nitrogen-containing gaseous atmosphere.

19. The process according to claim 18, wherein the gaseous atmosphere includes at least one gas selected from

the group consisting of N_2O, NO or NH_3.

20. The process according to claim 18, wherein the first region of semiconductor material is subjected to temperatures of about 300° C to about 1000° C.

21. The process according to claim 18, wherein the first region of semiconductor material is subjected to the elevated temperatures and gaseous atmosphere for a time of about 1 second to about 60 seconds.

22. The process according to claim 18, wherein the at least one region of dielectric material includes a discontinuous film of Si_xN_y, or $Si_xO_yN_z$.

23. The process according to claim 18, wherein the first region of semiconductor material is monocrystalline silicon.

24. The process according to claim 18, wherein exposing the first region of semiconductor material to the elevated temperatures includes ramping the temperature up a process temperature.

25. The process according to claim 24, wherein the temperature is ramped up at a rate of about 5° C per second to about 100° C per second to a temperature of about 400° C to about 800° C.

26. The process according to claim 24, wherein subjecting the first semiconductor material to a gaseous atmosphere includes subjecting the first semiconductor material to a NH_3 gas flowing at a rate of about 5 SLPM for about 5 to about 15 seconds.

27. The process according to claim 18, further comprising:

ramping down the temperature to ambient temperature after subjecting the first semiconductor material to elevated temperature.

28. The process according to claim 27, wherein the temperature is ramped down at a rate of about 15° C to about 30° C.

29. The process according to claim 24, further comprising:

ramping down the temperature to ambient temperature

after subjecting the first semiconductor material to elevated temperature.

30. The process according to claim 18, wherein the process creates a discontinuous layer of dielectric material having a thickness of about 1 Å to about 10 Å on the first region of semiconductor material.

31. The process according to claim 18, further comprising:

depositing a second region of semiconductor material on the first region of semiconductor material.

32. The process according to claim 30, further comprising:

removing portions of the dielectric material at least one of during and after deposition of the second region of semiconductor material.

33. The process according to claim 18, wherein the first region of semiconductor is exposed to elevated temperatures and nitrogen-containing gaseous atmosphere by a rapid thermal process or a conventional furnace process.

34. The process according to claim 1, wherein forming the at least one region of dielectric material comprises:

depositing a discontinuous film of the dielectric material by a chemical vapor deposition process.

35. The process according to claim 33, wherein the chemical vapor deposition process is a low pressure chemical vapor deposition process or a plasma enhanced chemical vapor deposition process.

36. The process according to claim 33, wherein the chemical vapor deposition process is carried out using silane or dichlorosilane with NH_3 or N_2O.

37. The process according to claim 33, wherein the film has a thickness of about 1 Å to about 10 Å.

38. The process according to claim 33, wherein the film has a thickness of less than one monolayer.

39. The process according to claim 33, wherein the chemical vapor deposition is carried out at a temperature of about 600° C to about 800° C.

40. The process according to claim 33, wherein deposition gases flow for less than about 5 seconds.

41. The process according to claim 33, wherein the chemical vapor deposition process utilizes at least one silicon source gas and at least one nitrogen/oxygen source gas and a ratio of silicon source gas to nitrogen/oxygen source gas is controlled to produce a desired silicon-nitrogen/oxygen stoichiometry.

42. The process according to claim 1, wherein the at least one region of dielectric material is deposited on a sidewall of a trench.

43. The process according to claim 1, wherein the dielectric material further comprises at least one oxide.

44. A semiconductor device prepared by a process comprising:

forming at least one region of dielectric material in the vicinity of at least a portion of a boundary between the two regions of semiconductor material, thereby controlling electrical resistance at the interface, the dielectric material including nitrogen.

45. A semiconductor device, comprising:

a region of a first semiconductor material;

a region of a second semiconductor material; and

an interface region including at least one region of dielectric material comprising nitrogen in the vicinity of at least a portion of a boundary between the first region of semiconductor material and the second region of semiconductor material, thereby controlling electrical resistance at the interface.

46. The semiconductor device according to claim 45, wherein the first region of semiconductor material and the second region of semiconductor material are selected from the group consisting of monocrystalline silicon, polycrystalline silicon, amorphous silicon, polycrystalline SiGe and monocrystalline SiGe.

47. The semiconductor device according to claim 45, wherein a first of the two regions of semiconductor material is monocrystalline silicon and a second of the regions of semiconductor material is non-monocrystalline silicon.

48. The semiconductor device according to claim 47, wherein the second region of semiconductor material is

amorphous silicon.

49. The semiconductor device according to claim 45, wherein the dielectric material is N, Si_xN_y, or $Si_xO_yN_z$.

50. The semiconductor device according to claim 45, wherein the dielectric material is implanted at the surface of the first region of semiconductor material.

51. The semiconductor device according to claim 45, wherein atoms of the dielectric material are implanted at the surface of one of the regions of semiconductor material.

52. The semiconductor device according to claim 45, wherein atoms of the dielectric material are implanted under the surface of one of the regions of semiconductor material.

53. The semiconductor device according to claim 45, wherein one of the regions of semiconductor material is monocrystalline silicon and the dielectric material includes nitrogen atoms implanted in the monocrystalline silicon.

54. The semiconductor device according to claim 45, wherein the at least one region of dielectric material is a

discontinuous film.

55. The semiconductor device according to claim 54, wherein the film is silicon nitride or silicon oxynitride.

56. The semiconductor device according to claim 54, wherein the film of dielectric material has a thickness of about 1 Å to about 10 Å.

57. The semiconductor device according to claim 54, wherein the film of dielectric material has a thickness of less than one monolayer.

58. The semiconductor device according to claim 45, wherein the at least one region of dielectric material is arranged on a sidewall of a trench in monocrystalline silicon, the trench being filled with non-monocrystalline silicon.

59. The semiconductor device according to claim 45, wherein the dielectric further comprises at least one oxide.